

FIGURE 1A

FIG. 1B

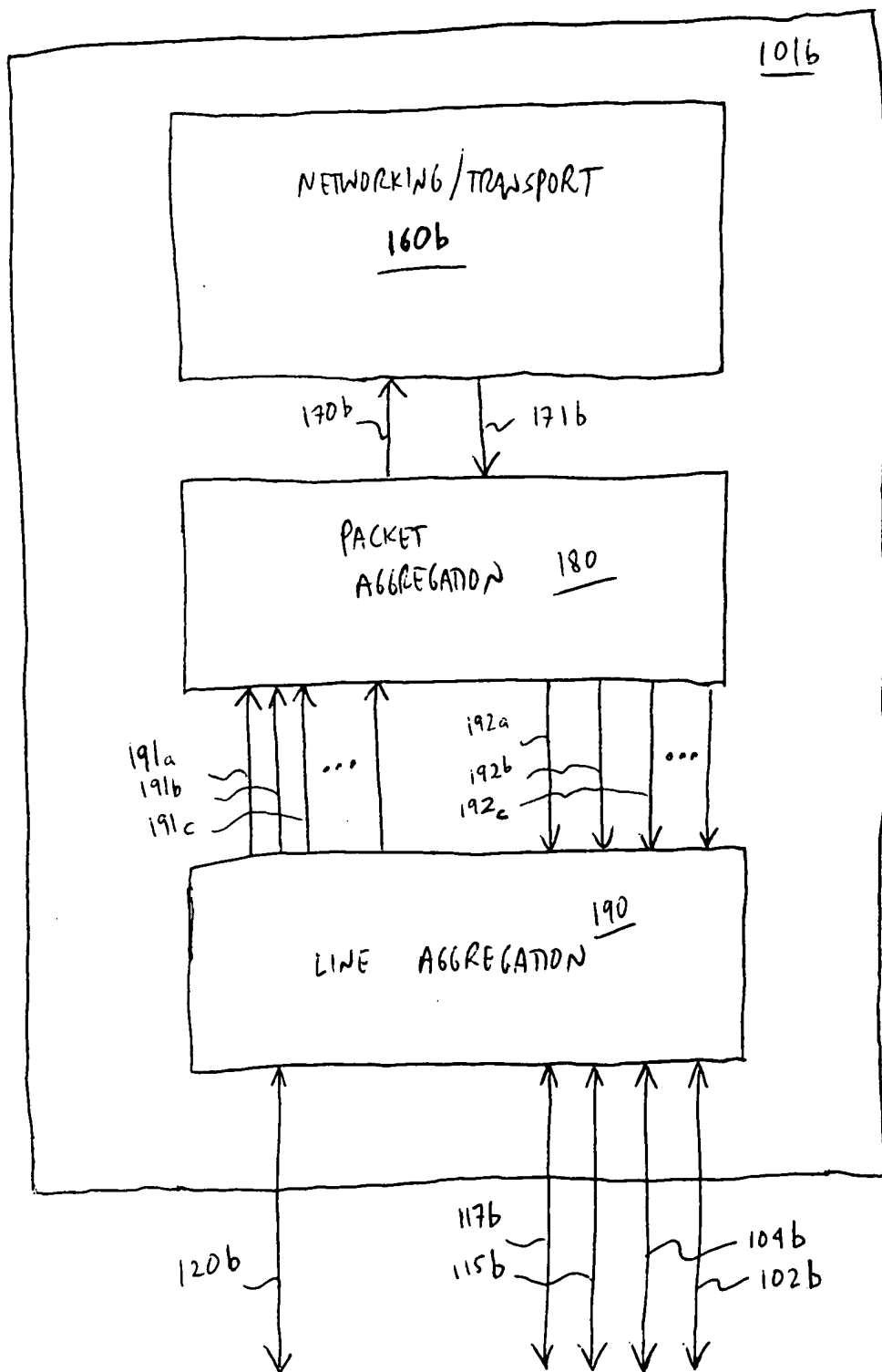


FIGURE 1B

TOP SECRET

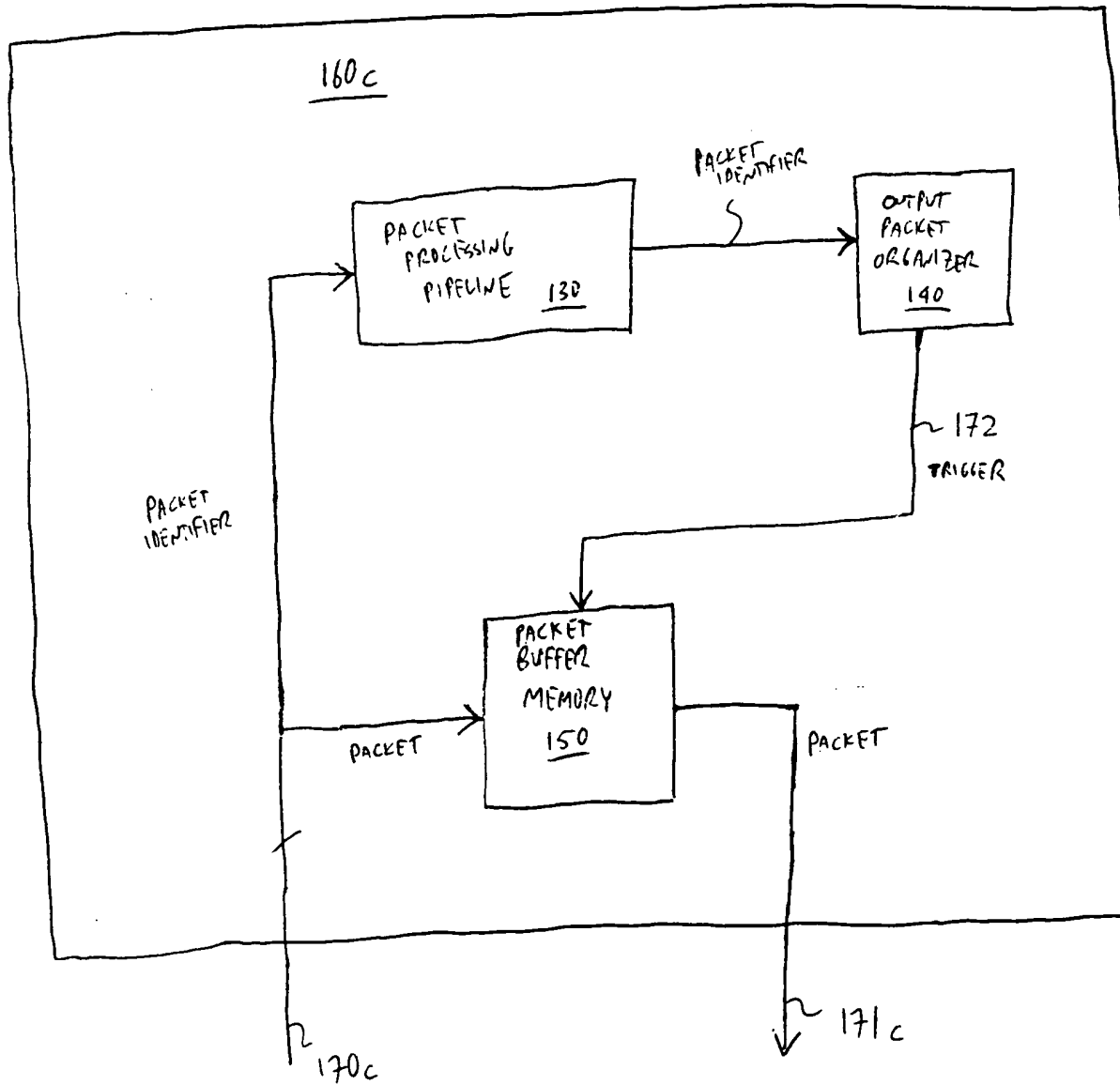
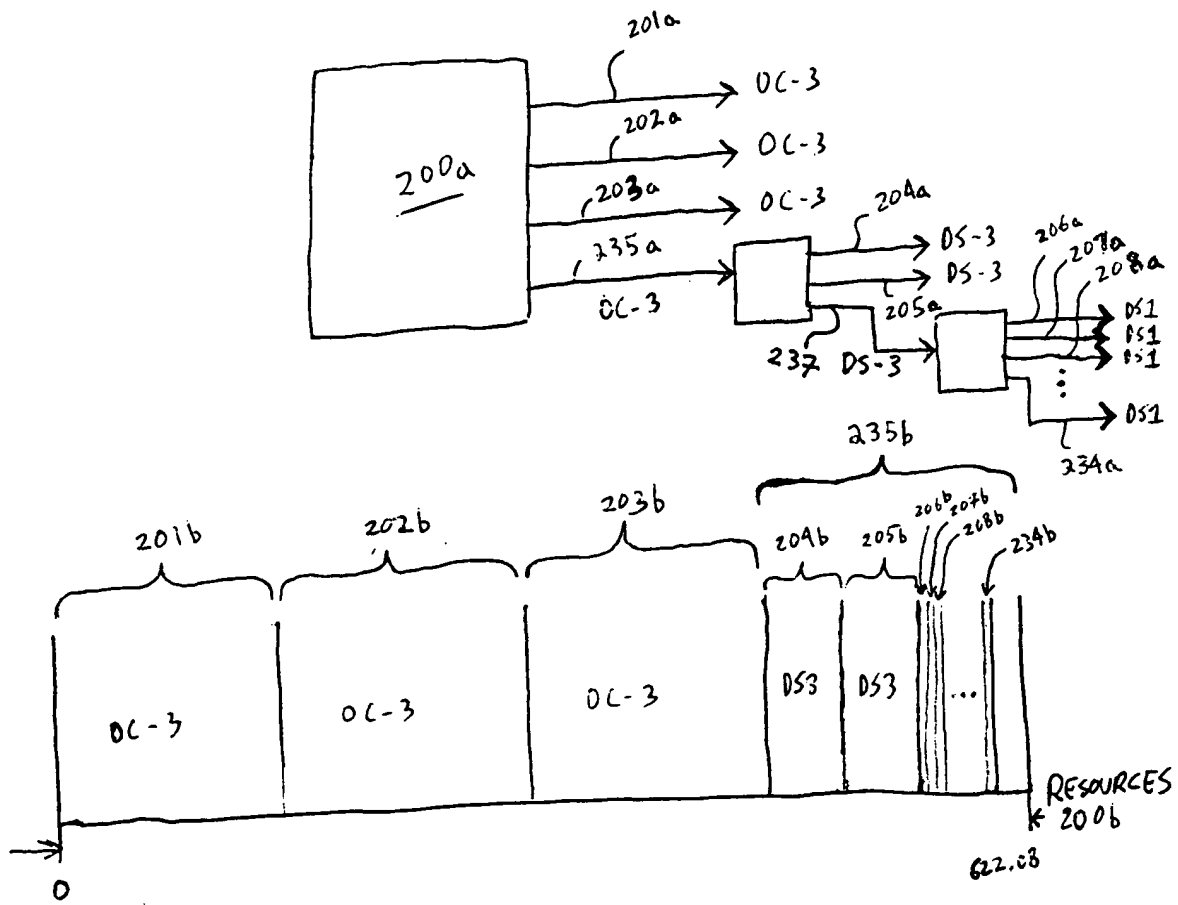


FIGURE 1c

FIGURE 2



Mb/s

FIGURE 2

TOO LONG TO SEE

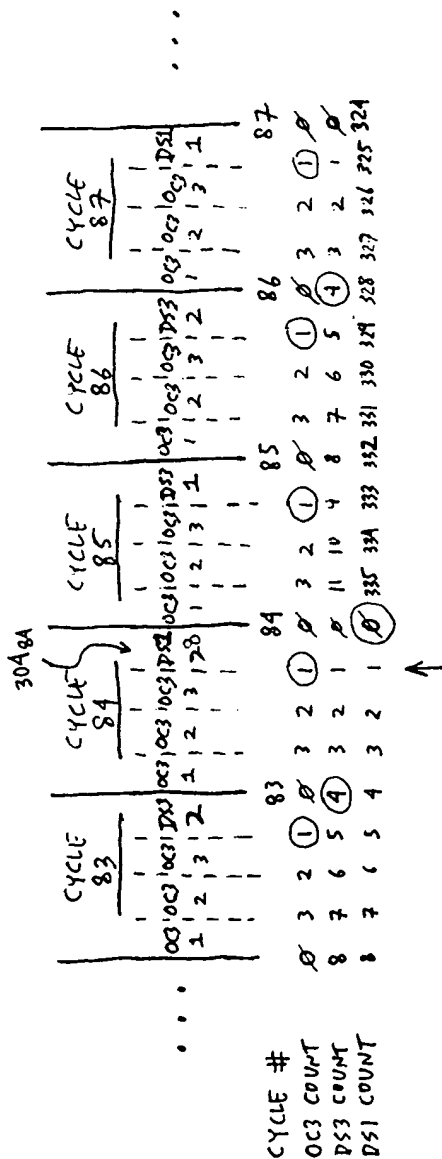
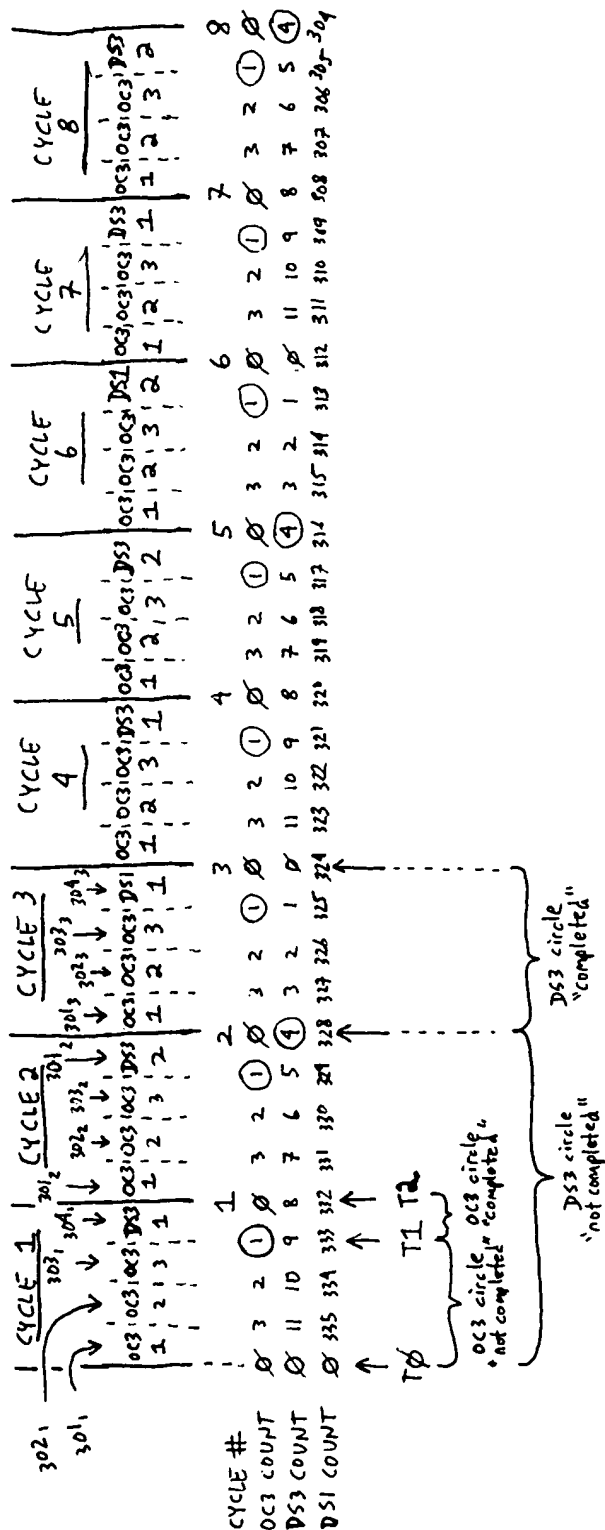


FIGURE 3

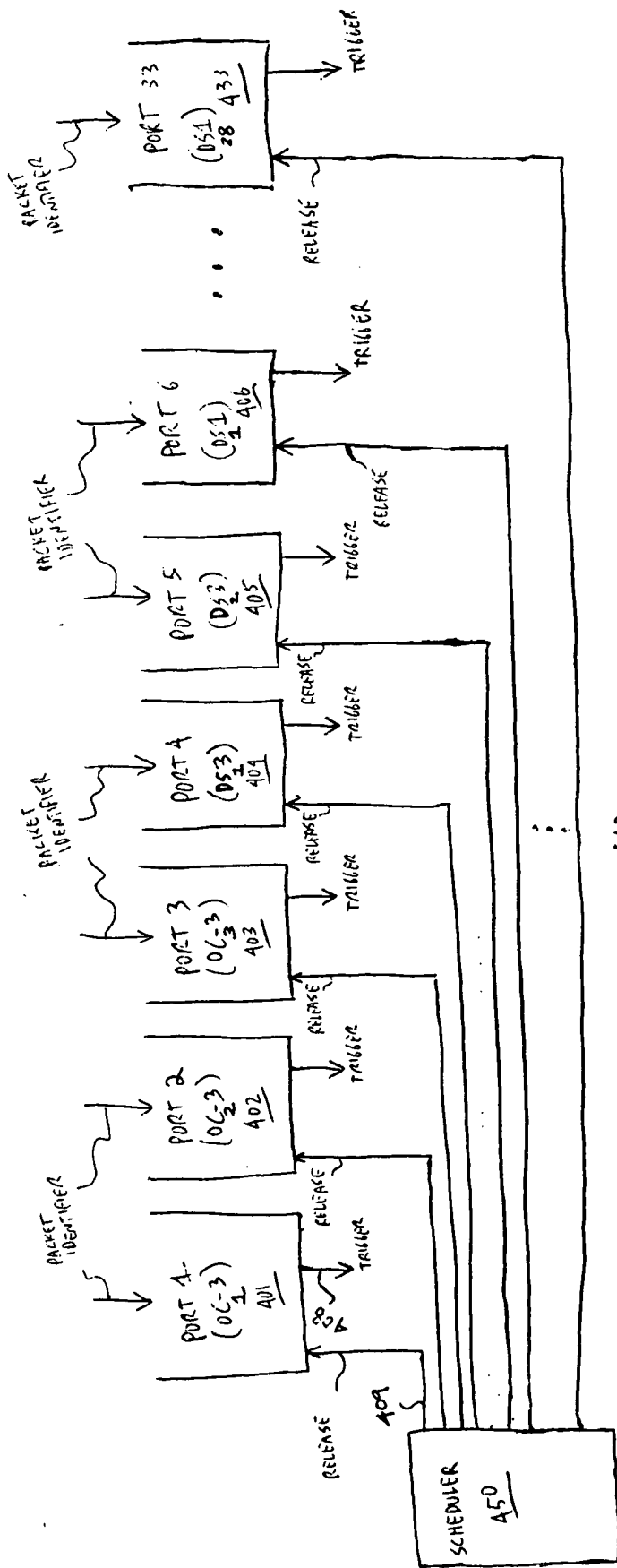


FIGURE 4

500a

	DATA ENTRY				
	ADDR	LINK POINTER	PID	DONE BIT	
PORT 1	501	502	PID ₁	0	OC3_1
PORT 2	502	503	PID ₂	0	OC3_2
PORT 3	503	501	PID ₃	1	OC3_3
PORT 4	504	505	PID ₄	0	DS3_1
PORT 5	505	504	PID ₅	1	DS3_2
PORT 6	506	507	PID ₆	0	DS1_1
PORT 7	507	508	PID ₇	0	DS1_2
PORT 32	532	533	PID ₃₂	0	DS1_27
PORT 33	533	506	PID ₃₃	1	DS1_28

FIG. 5A

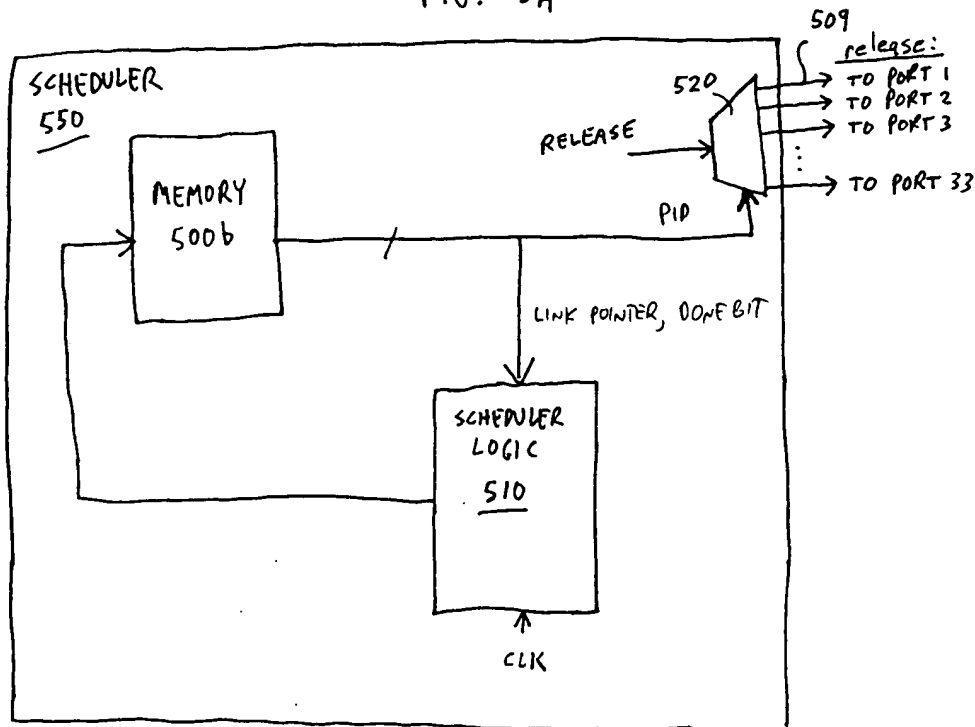


FIG. 5B

FIG. 5A

FIGURE 6

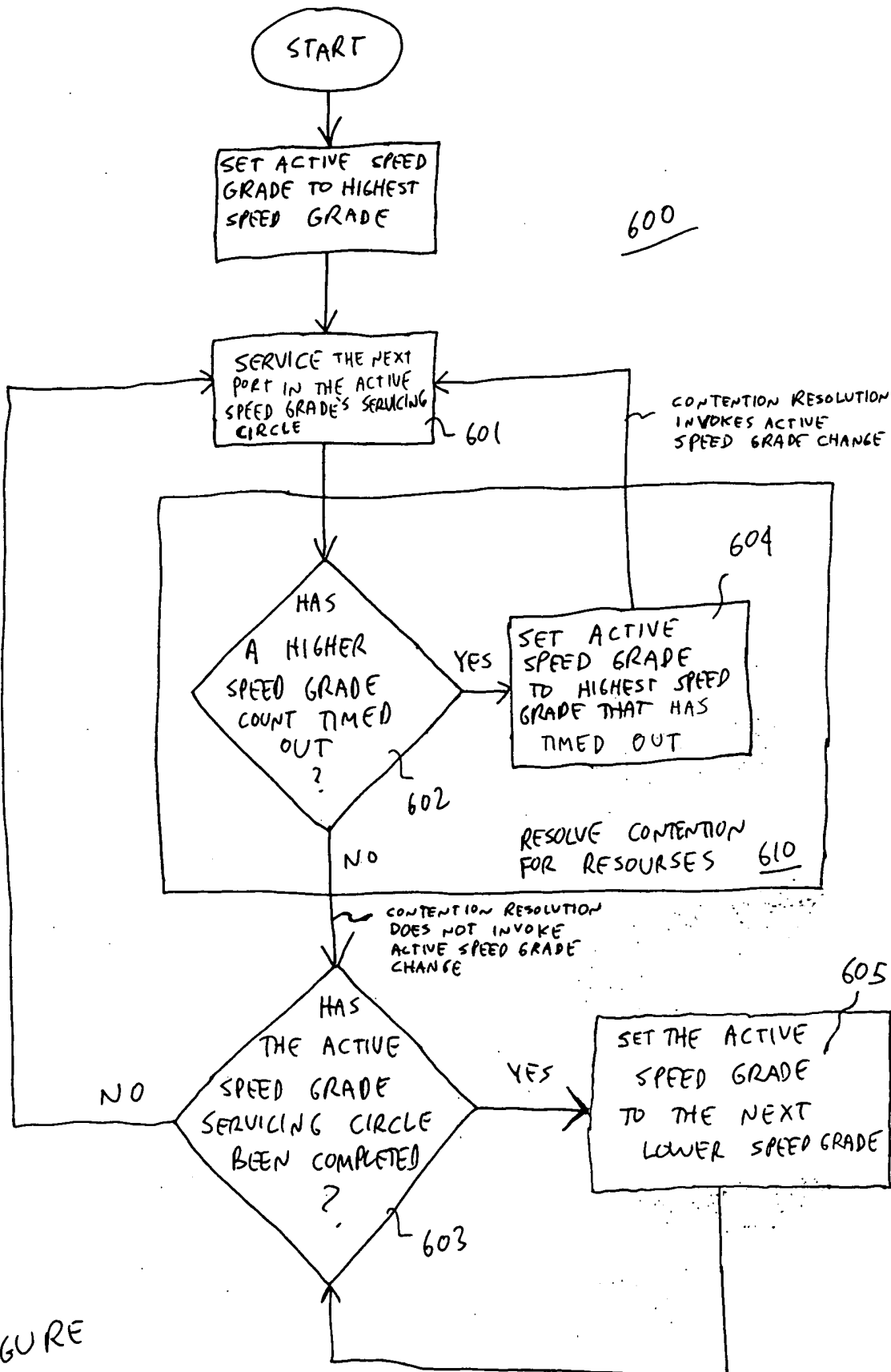
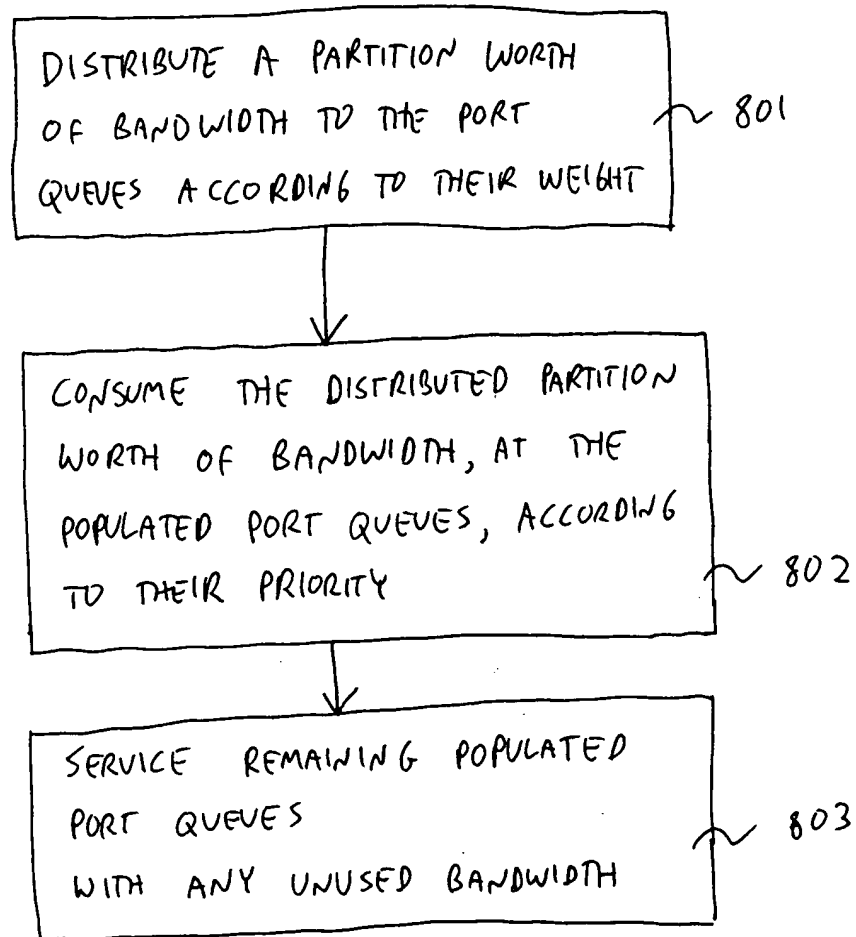


FIGURE 6

Hand-drawn block diagram of a packet scheduling system (700) for PORT X. The system includes a QUEUE SCHEDULER (706) and five queues (701-705). Load credits (709) enter the scheduler. Packet identifiers (707) enter the queues. Weights (WT₁-WT₅) are assigned to each queue. The scheduler outputs packet identifiers (708) and triggers (708) to the queues. The queues output packet identifiers (708) and triggers (708) to the output. The scheduler also outputs a release signal (709) to the queues.

FIGURE 7



800

FIGURE 8

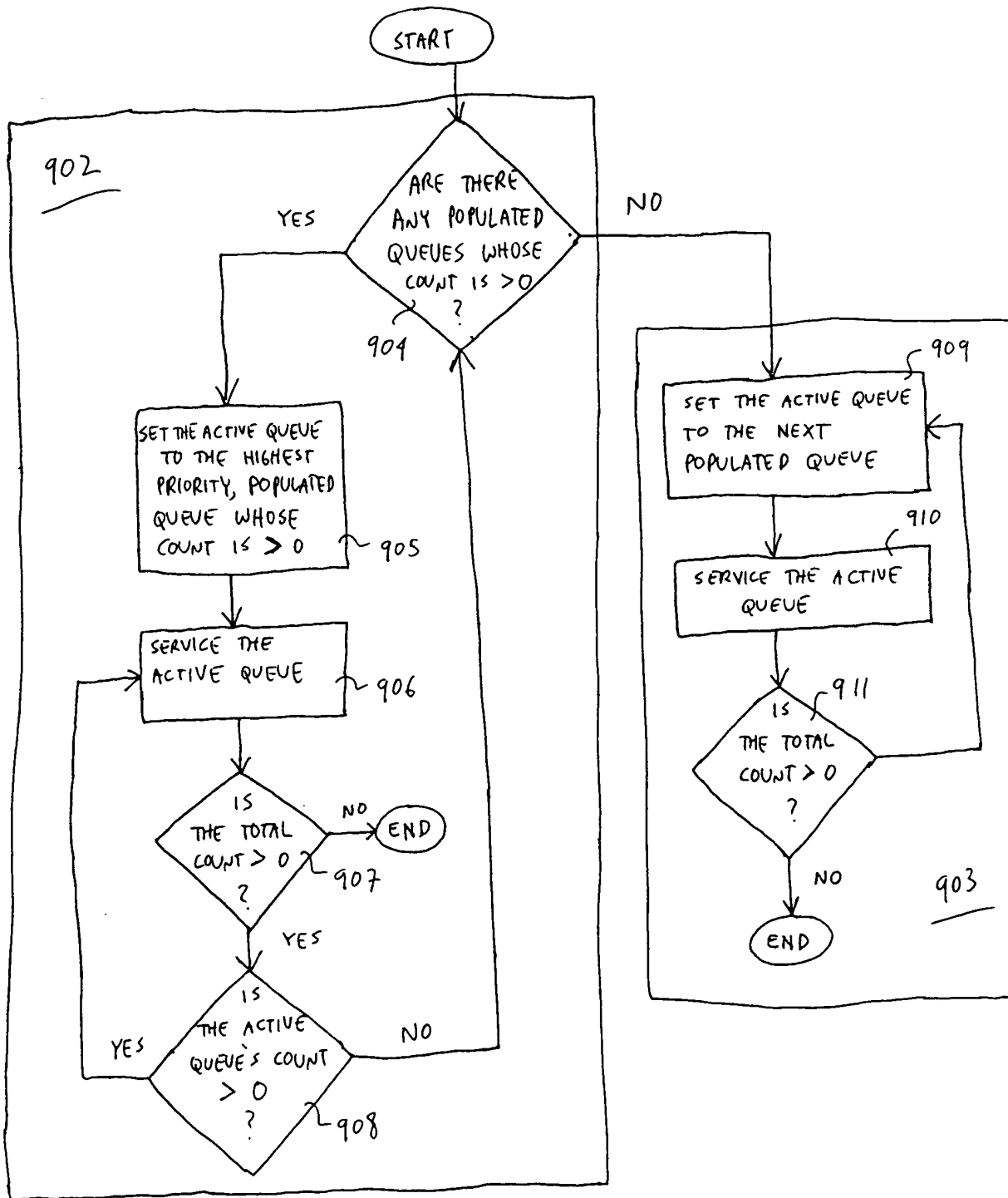


FIGURE 9